

Aliasing errors in linear automata used as multiple-input signature analyzers

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This paper deals with the aliasing probability of multiple-input data compressors used in self-testing networks. It is shown that a far more general class of linear machines than linear feedback shift registers can be used for data compression purposes. The function of these machines is modeled by a Markov process. The steady-state value of the aliasing probability is shown to be the same as for single-input signature analysis registers. An easily verifiable criterion is given that allows one to decide whether a given linear machine falls into this class of multiple-input data compressors. The steady-state value of the aliasing probability is shown to be independent of the correlation of

the data streams at the inputs of the data compressor. Two kinds of circuits are analyzed in more detail with respect to their aliasing properties: linear feedback shift registers with multiple inputs, and linear cellular automata. Simulation results show the effect of the next-state function on the steady-state value of the aliasing probability and the effect of correlation on the transient response.

Introduction

With the use of signature-analysis techniques for testing boards introduced by Hewlett Packard [1], considerable attention has been paid to the aliasing problem—i.e., what is the probability that faulty test responses cannot be distinguished in the signature analysis register? The structure shown in **Figure 1** is an example of a signature analysis register. The network is supplied with a pattern, and the network responds with a single output which goes into the first exclusive-OR gate. The output of this exclusive-OR gate then feeds a shift register of length k . The second and the last bits of the shift register are

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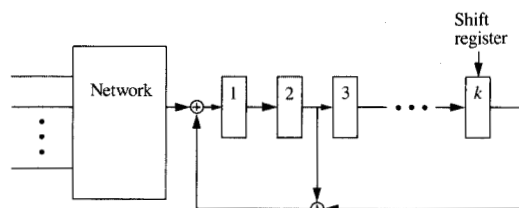


Figure 1

Signature analysis register.

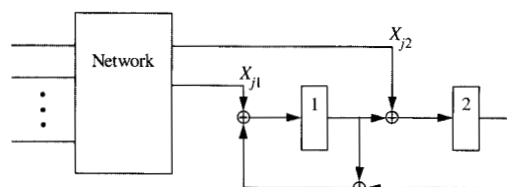


Figure 2

Multiple-input signature analysis register.

exclusive-ORed and are fed back to the input side of the shift register. Before a test is begun, the shift register is initialized to a given value. Let us assume that the network is combinational, so that we need not deal with the initialization of the network under test.

Patterns are applied to the network synchronously with the shifting of the shift register. A test pattern is applied to the network inputs. The response produced at the network output is shifted one bit position into the shift register, concurrent with the application of a new test pattern. As a result, a new value resides in the shift register, it is ready to accept its next value from the output of the network, and so on.

Before the aliasing can be discussed in detail, a few comments about probability must be made relative to this type of structure. Consider the network in Figure 1, and assume that there is a defect in the network such that (at least for one pattern) the output is different from the good-machine response. Given this defect in the network, assume that all possible patterns are applied to this network, and the network's output is observed. Of all the

2^n patterns, where n is the number of inputs to the network, assume that there are exactly m patterns which are different from those of the good machine. Thus, if an input vector for the network is selected randomly from the set of all possible input vectors, the probability that the output of the network is correct is $m/2^n$.

Thus, for this network and this defect we can say that for a random vector the probability of getting an incorrect output is p , where p is $m/2^n$. If the input vectors are always selected from the space of all possible vectors, the probability of an incorrect output will always be p for this defect. For a stuck-at fault which is testable (i.e., there exists at least one input vector such that the good-machine response is different from the faulty-machine response), we can also say that given a random pattern, the probability of having a different output is p , where this p is calculated in the same manner as above. Hence, if a stuck-at fault or a particular defect is being discussed, we can associate with it a parameter p to describe the probability of an incorrect output of the network under consideration. We also may refer to this less formally as the probability of an error in the output of the network, or simply the probability of an error.

We define the probability of aliasing to be the probability of all possible faulty test responses which cannot be differentiated from the defect-free response (due to the loss of information in response compaction).

There are many forms of this kind of testing, from transition counting to syndromes, signature analysis, parity bits, etc. [2-7]. Linear feedback shift registers (LFSRs) have been proposed to be an integral part of the sequential logic design so that they can be used to both generate and compact the results of a test [8, 9]. With respect to hardware overhead, this solves the problems of test data storage for BIST [10, 11]. Instead of storing test stimuli and test responses in an additional on-chip ROM, LFSRs could be used to generate pseudorandom patterns that exercise the network. Test-response compaction by LFSRs permits the mapping of network test responses onto a single data word, eliminating the need for storing thousands of expected test responses for on-chip comparison with the measured data. The signature registers suggested in [9] are different from the one shown in Figure 1, in that they may have more than one input (see Figure 2). Such registers are known as multiple-input signature analysis registers (MISRs). In prior work, considerable attention has been paid to the bounds and final values of aliasing in signature analysis registers such as those shown in Figure 1 [12-22]. In those papers which mention multiple-input signature analysis, this case is treated by alluding to superposition or by restricting either the type of signature analysis register or the type of allowable faulty output [23]. However, none give the final value of aliasing, nor do they discuss what

happens when different, possibly correlated, error probabilities are introduced to the different inputs of the shift register.

This work addresses the aliasing problem in a more general way by treating multiple-input signature analysis registers as a special kind of linear data compressor [24, 25]. The analysis also considers a modification of LFSRs recently presented at the 1989 European Test Conference [26].

First, two theorems are presented which show the final value for aliasing when each input bit to each input stage has a probability p of an error and these errors are independent. The results are also given for the case when the probabilities of error for each of the inputs are different from one another but still independent. The analysis is based on the Markov model of the process [14, 16, 20]. A number of simulation results are given to demonstrate the conclusions.

Next, correlation is allowed between data streams which are inputs to the multiple-input data compressor. Given this type of input, a sufficient condition for the type of feedback network is found, such that the final value of the probability of aliasing is 2^{-k} , where k is the number of bits in the register. With these results, a new class of data compressors is defined. Again, simulations reinforcing the results are given for multiple-input signature analysis registers and cellular automata with correlated inputs.

Notation and definitions

Before proceeding to investigate linear data compressors, a notation for MISRs is derived. It is then shown that this notation is also adequate to describe a more general class of linear data compressors. Figure 3 shows a general form of a multiple-input signature analysis register with a linear feedback function. It is linear because all the elements of the feedback function are exclusive-ORs which are linear elements over the field GF(2).

The operation of the MISR of length k can be described in matrix notation. The state of the register can be represented by a column vector,

$$Y(t) = [y_1(t), y_2(t), \dots, y_k(t)]^T,$$

and the input at time t can be represented by a column vector,

$$X(t) = [x_1(t), x_2(t), \dots, x_k(t)]^T.$$

The next state of the register is calculated by multiplying the current state vector by a next-state matrix C and adding the current input to the product. The first row of the matrix C is defined by the presence or absence of feedback taps of the given shift register. The next $k-1$ rows represent the shifting function of the shift register. This is accomplished by setting the lower off-diagonal

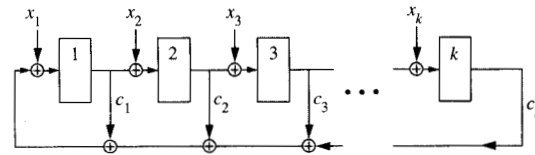


Figure 3

General structure of a multiple-input signature analysis register.

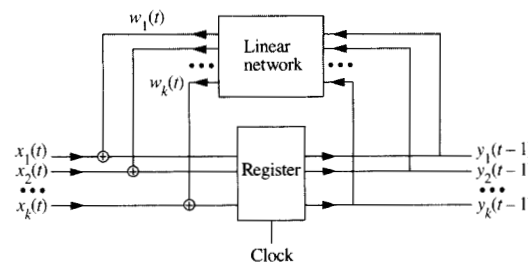


Figure 4

Structure of a linear data compressor.

elements to one and all other elements to zero, as shown in the following equation:

$$\begin{bmatrix} y_1(t) \\ y_2(t) \\ y_3(t) \\ \vdots \\ y_k(t) \end{bmatrix} = \begin{bmatrix} c_1 & c_2 & c_3 & \dots & c_k \\ 1 & 0 & 0 & \dots & 0 \\ 0 & 1 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & 1 \end{bmatrix} \cdot \begin{bmatrix} y_1(t-1) \\ y_2(t-1) \\ y_3(t-1) \\ \vdots \\ y_k(t-1) \end{bmatrix} \oplus \begin{bmatrix} x_1(t) \\ x_2(t) \\ x_3(t) \\ \vdots \\ x_k(t) \end{bmatrix}.$$

$$Y(t) = C \cdot Y(t-1) \oplus X(t).$$

Remember that all additions are done modulo 2.

We now use this matrix notation to describe a more general class of linear automata than LFSRs.

The general structure of the investigated data compressors is shown in Figure 4. It is a special case of a general linear sequential machine [2]. The input vector $X(t)$ feeds the modulo 2 adder directly at the register inputs, and the state of the machine is directly observable. The data compressor consists of a synchronously clocked register, a linear feedback network, and k bitwise modulo 2 adders. The next state,

$y_i(t)$, of a given register position is the sum of the input bit $x_i(t)$ and $w_i(t)$, which is calculated as a linear combination of the values $y_j(t-1)$, $j = 1, \dots, k$, of the previous state. The values of all variables y_j , w_i , and x_i are elements of GF(2), and addition is performed modulo 2 (XOR-operation). The above structure for a data compressor has been chosen because of its ease of implementation in a BIST environment. The register can be built from existing output latches of the network, and only a small amount of hardware for the feedback network and the k modulo 2 adders must be added to a given design.

Again, the operation of the data compressor can be described by the following matrix equation:

$$Y(t) = C \cdot Y(t-1) \oplus X(t).$$

The matrix C describes the function of the feedback network, which is allowed to be significantly more complex than in the LFSR case. Each bit $w_i(t)$ can be an arbitrary linear combination of the bits of the previous state vector $Y(t-1)$. If the initial state of the data compressor is $Y(-1)$, the state at time j can be calculated using the above recursion formula in the following way:

$$Y(0) = C \cdot Y(-1) \oplus X(0),$$

$$Y(1) = C \cdot Y(0) \oplus X(1)$$

$$= C^2 \cdot Y(-1) \oplus C \cdot X(0) \oplus X(1),$$

$$Y(2) = C \cdot Y(1) \oplus X(2)$$

$$= C^3 \cdot Y(-1) \oplus C^2 \cdot X(0) \oplus C \cdot X(1) \oplus X(2),$$

...

$$Y(j) = C^{j+1} \cdot Y(-1) \oplus \sum_{i=0}^j C^{j-i} \cdot X(i).$$

The state of the data compressor at time j is a linear combination of the input vector sequence X and the initial condition $Y(-1)$. This state will be referred to as the signature.

Let us now assume that a sequence X' is applied to the data compressor. X' is defined as the modulo 2 sum of the good-machine output sequence X and an error sequence $E(t) = [e_1(t), e_2(t), \dots, e_k(t)]^T$:

$$X'(t) = X(t) \oplus E(t) \quad \text{for } 0 \leq t \leq j.$$

An element $e_i(t)$, $i = 1, \dots, k$, of the error vector $E(t)$ is 1 whenever there is a difference between the good-machine response and the faulty-machine response at output i . For X' , the following signature Y' of a faulty network is obtained:

$$\begin{aligned} Y'(j) &= C^{j+1} \cdot Y(-1) \oplus \sum_{i=0}^j C^{j-i} \cdot X'(i) \\ &= C^{j+1} \cdot Y(-1) \oplus \sum_{i=0}^j C^{j-i} \cdot [X(i) \oplus E(i)] \\ &= [C^{j+1} \cdot Y(-1) \oplus \sum_{i=0}^j C^{j-i} \cdot X(i)] \\ &\quad \oplus \sum_{i=0}^j C^{j-i} \cdot E(i), \\ Y'(j) &= Y(j) \oplus \sum_{i=0}^j C^{j-i} \cdot E(i) = Y(j) \oplus Y_e(j). \end{aligned}$$

Thus, for all linear data compressors of the general structure shown in Figure 4, the signature of a faulty machine equals the signature of the good machine plus the summation associated with the error sequence. Moreover, $Y_e(j)$ is independent of the good-machine response. We therefore assume without loss of generality that the initial state $Y(-1)$ of the data compressor is always logical zero and that the good-machine response is an all-zero sequence:

$$Y(-1) = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix}; \quad X(t) = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad \text{for all } t.$$

With this assumption, aliasing is characterized by a data compressor starting in the "all-zero" state, $Y(0) = '0'$, and returning to that state if the error sequence is applied and if there is at least one nonzero element in the error sequence.

Aliasing and Markov processes

A Markov process is represented in a manner very similar to that used to describe sequential machines. As with sequential machines, a Markov process is defined in terms of states and transitions. Figure 5 shows the transition diagram of a 2-bit multiple-input signature analysis register. The arcs are labeled by the input symbol which results in the associated transition. When the input sequence to the signature analysis register is random, the transitions are done with the probabilities of the respective input symbols. By replacing the input symbols with their probabilities, the transition diagram for the Markov process describing the operation of the signature analysis register with random signals at the input is obtained.

Let p_{ij} be the probability of going from state i of the register to state j of the register in one step, and, further, let p_{ij} be constant (this is called the Markov property). That is, no matter what time one enters state i , the probability of going to state j is always p_{ij} . A Markov

process on the $n = 2^k$ possible states can be described by the transition matrix $\mathbf{P} = (p_{ij})$. Let $\pi(0) = [\pi_1(0), \pi_2(0), \dots, \pi_n(0)]$ be the initial condition vector for the state of the Markov process. Thus, $\pi_i(0)$ is the probability that one starts in state i of the register at time 0. We arbitrarily assign state 1 to the all-zero ('0') state.

Given the vector $\pi(0)$ of initial state probabilities $\pi_i(0)$, the probability of a data compressor being in some state i at time j can be calculated by the following matrix equation:

$$\pi(1) = \pi(0) \cdot \mathbf{P},$$

$$\pi(2) = \pi(1) \cdot \mathbf{P} = \pi(0) \cdot \mathbf{P}^2,$$

...

$$\pi(j) = \pi(0) \cdot \mathbf{P}^j.$$

Consider the probability of the data compressor starting in the all-zero state and returning to it after j cycles. The initial state probabilities $\pi_i(0)$ must all be set to zero except for the all-zero state, whose probability $\pi_1(0)$ is one. The aliasing probability is obtained by excluding the case of an all-zero error sequence:

$$Pr_{al}(j)$$

$$= Pr[Y(j) = '0' / Y(0) = '0'] - Pr[E(t) = [0, 0, \dots, 0]$$

$$\text{for } t = 0, \dots, j]$$

$$= \pi_1(j) - Pr[E(t) = [0, 0, \dots, 0]$$

$$\text{for } t = 0, \dots, j].$$

Let the probability that $E(t) = [0, 0, \dots, 0]$ be q ; then, the probability that $E(t) = [0, 0, \dots, 0]$ for $t = 0, \dots, j$ is q^{j+1} . Thus,

$$\lim_{j \rightarrow \infty} Pr[E(t) = [0, 0, \dots, 0] \text{ for } t = 0, \dots, j]$$

$$= \lim_{j \rightarrow \infty} q^{j+1} = 0.$$

Therefore, in investigating the steady-state value of Pr_{al} we need to find only the steady-state value of $\pi_1(j)$, which is

$$\lim_{j \rightarrow \infty} \pi_1(j) = \pi_1.$$

For ergodic Markov processes [24, 25, 28] with a doubly stochastic transition matrix $\mathbf{P}$, the value of π_1 can be calculated easily. A Markov process is ergodic if there is a finite number of time steps such that the probability of a transition from any state to any other state is greater than zero. A transition matrix of a Markov process is called doubly stochastic if the sum of the elements of every row is one and if the sum of the elements of every column is one. For an ergodic Markov process with n

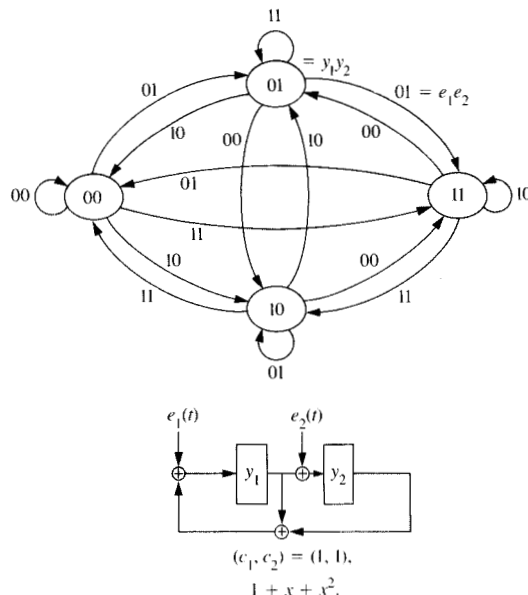


Figure 5

State transition diagram for the multiple-input signature analysis register with feedback function $1 + x + x^2$.

states and with a doubly stochastic transition matrix, the final value of the state probability $\pi_i(t)$ will be the same for all states [28]. Thus,

$$\lim_{j \rightarrow \infty} \pi_i(j) = 1/n \quad \text{for all } 1 \leq j \leq n,$$

and

$$\lim_{j \rightarrow \infty} Pr_{al}(j) = 1/n = 2^{-k}.$$

We now investigate the conditions under which the Markov process is ergodic and has a doubly stochastic transition matrix.

Let us start by using a single-input signature analysis register as a small example. For a single-input signature analysis register of length k , we have the following equation:

$$\begin{bmatrix} y_1(t) \\ y_2(t) \\ y_3(t) \\ \vdots \\ y_k(t) \end{bmatrix} = \begin{bmatrix} c_1 & c_2 & c_3 & \dots & c_k \\ 1 & 0 & 0 & \dots & 0 \\ 0 & 1 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & 1 \end{bmatrix} \begin{bmatrix} y_1(t-1) \\ y_2(t-1) \\ y_3(t-1) \\ \vdots \\ y_k(t-1) \end{bmatrix} \oplus \begin{bmatrix} x_1(t) \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix}.$$

Given a present-state vector $Y(t) = [y_1(t), \dots, y_k(t)]^T$, we must show first that it has exactly two possible predecessor states, and that together the transitions from

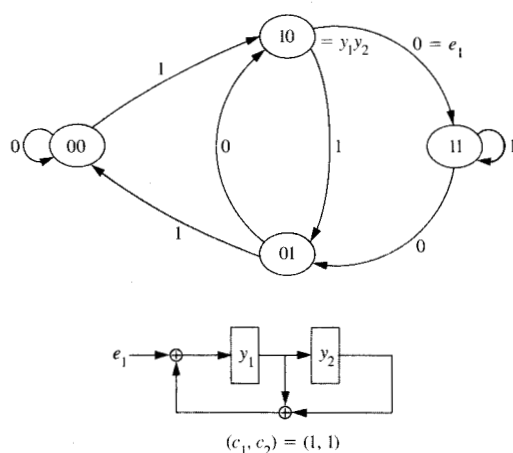


Figure 6

State transition diagram for the single-input signature analysis register with feedback function $1 + x + x^2$.

these states to the present state have probability one. If we can do this, we will be able to show that the matrix is doubly stochastic. From the fact that the basic structure is a shift register, which is reflected by the off-diagonal ones in the above equation, we immediately get

$$y_i(t) = y_{i-1}(t-1), \quad i = 2, 3, \dots, k.$$

Thus, we must try to find a $y_k(t-1)$ that satisfies the general equation; if so, we must determine the number of possible values of $y_k(t-1)$. From the general equation above, we have

$$\begin{aligned} y_1(t) &= \sum_{i=1}^k c_i \cdot y_i(t-1) \oplus x_1(t) \\ &= \sum_{i=1}^{k-1} c_i \cdot y_i(t-1) \oplus c_k \cdot y_k(t-1) \oplus x_1(t), \end{aligned}$$

and making the substitutions for $y_i(t-1)$,

$$y_1(t) = \sum_{i=1}^{k-1} c_i \cdot y_{i+1}(t) \oplus c_k \cdot y_k(t-1) \oplus x_1(t).$$

Since $c_k = 1$,

$$y_1(t) = \sum_{i=1}^{k-1} c_i \cdot y_{i+1}(t) \oplus y_k(t-1) \oplus x_1(t).$$

Solving for $y_k(t-1)$,

$$y_k(t-1) = y_1(t) \oplus \sum_{i=1}^{k-1} c_i \cdot y_{i+1}(t) \oplus x_1(t).$$

There are thus two possible solutions for $y_k(t-1)$ from

the above equation: one solution when $x_1(t) = 1$, which happens with probability p , and one solution when $x_1(t) = 0$, which happens with probability $1 - p$. Since this is true for any given state, $Y(t)$, we have that the elements of each column of the transition matrix sum to one, or

$$\sum_{i=1}^{2^k} p_{ij} = 1.$$

The elements of the rows of the transition matrix of the Markov process are the probabilities of making a transition from state i to some state j of the register. This can happen in two ways, by inserting a one into the signature analysis register with probability p , or by inserting a zero with probability $1 - p$. Thus, the elements of every row sum to 1. The transition matrix therefore has the property that it is doubly stochastic; i.e., both the elements of every row and the elements of every column sum to one. Furthermore, since it is possible to get from any state to any other state if $p \neq 0, 1$ in k (or more) steps, the system is irreducible and has a unique stationary solution $\pi = [2^{-k}, 2^{-k}, \dots, 2^{-k}]$ such that

$$\pi = \pi \cdot P,$$

and we have the following theorem.

Theorem 1

Given $p \neq 0, 1$ and $c_k = 1$, then the final probability of being in any of the 2^k states of a k -length signature analysis register is $1/2^k$, regardless of the initial condition.

This theorem holds for any signature analysis register, provided that the feedback function includes the last bit of the shift register.

Using the above line of reasoning,

$$\lim_{j \rightarrow \infty} Pr_{al}(j) = \lim_{j \rightarrow \infty} \pi_1(j) = 2^{-k},$$

we obtain the following corollary.

Corollary The final value of the probability of aliasing Pr_{al} in a signature analysis register of length k with $c_k = 1$ is $1/2^k$, irrespective of the error detection probability p , $0 < p < 1$.

If the same theorem (doubly stochastic) can be proven for multiple-input signature analyzers, we will have shown that they converge to an aliasing probability of $1/2^k$. Thus, we need to show that the transition matrix $P = (p_{ij})$ for the Markov process for the register with multiple inputs is also doubly stochastic. First, let us examine how a transition matrix for a single-input signature analysis register differs from a transition matrix for a multiple-input signature analysis register. We are using the multiple-input signature analysis register shown

in Figure 5, with states 00, 01, 11, 10 represented by subscripts 1, 2, 3, 4 of the elements of the transition matrix. The following is the transition matrix for the single-input signature analysis register shown in Figure 6:

$$\begin{bmatrix} (1-p) & 0 & 0 & p \\ p & 0 & 0 & (1-p) \\ 0 & (1-p) & p & 0 \\ 0 & p & (1-p) & 0 \end{bmatrix}.$$

The following is the transition matrix for the multiple-input signature analysis register with the same polynomial shown in Figure 5:

$$\begin{bmatrix} (1-p)(1-p) & (1-p)p & pp & p(1-p) \\ p(1-p) & pp & (1-p)p & (1-p)(1-p) \\ (1-p)p & (1-p)(1-p) & p(1-p) & pp \\ pp & p(1-p) & (1-p)(1-p) & (1-p)p \end{bmatrix}.$$

These transition matrices for the two Markov processes are both doubly stochastic. We are now ready to prove the two theorems necessary to reach our goal.

Theorem 2

For any Markov process, the elements of every row of the transition matrix $\mathbf{P}$ sum to 1.

Proof See [28].

To be doubly stochastic, in addition to the elements of the rows, the elements of every column of the transition matrix must sum to 1. The following theorem relates properties of the next-state matrix of the data compressor and the transition matrix of the Markov process that models its behavior.

Theorem 3

If the determinant of the next-state matrix $\mathbf{C}$ of the data compressor is 1, the columns of the transition matrix $\mathbf{P}$ sum to 1.

Proof We show that for each state $Y_j(t)$ and each input symbol $X(t)$ there is a unique predecessor state $Y_i(t-1)$ of the data compressor iff the determinant of the next-state matrix $\mathbf{C}$ is one. Thus, the sum over all entries in a column of the transition matrix $\mathbf{P}$ will equal the sum over the probabilities of the input symbols X :

$$\sum_{i=1}^n p_{ij} = \sum_X p(X) = 1.$$

The proof is by construction:

$$Y_j(t) = \mathbf{C} \cdot Y_i(t-1) \oplus X(t),$$

$$Y_j(t) \oplus X(t) = \mathbf{C} \cdot Y_i(t-1).$$

If $|\mathbf{C}| \neq 0$, then $\mathbf{C}^{-1}$ exists, and

$$Y_i(t-1) = \mathbf{C}^{-1} \cdot [Y_j(t) \oplus X(t)].$$

Using Theorem 3, we can now identify which linear data compressors are good candidates for having an aliasing probability of 2^{-k} .

Corollary Provided the Markov process is ergodic, the final value of the aliasing probability of a linear data compressor with register length k is 2^{-k} if $|\mathbf{C}| = 1$.

Note that no assumptions have been made with respect to the probabilities of the input symbols X or the error symbols $E = (e_1, e_2, \dots, e_k)$. Thus, the results also hold if the error bits $e_i(t)$ are strongly correlated.

Clearly, if $0 < \Pr(e_1, e_2, \dots, e_k) < 1$ for all possible error patterns, then there exists a path between any pair of states Y_i and Y_j , and the Markov process is ergodic.

Theorem 4

If $0 < \Pr(E) < 1$ for all possible error patterns and if $|\mathbf{C}| = 1$, then the final value of the aliasing probability is

$$\lim_{j \rightarrow \infty} \Pr_{\text{al}}(j) = 2^{-k}$$

for a linear data compressor with a register of length k .

Before proceeding with the investigation of nonergodic Markov processes and deriving additional checking criteria, let us investigate the implication of the above result on the aliasing properties of multiple-input signature analysis registers and linear cellular automata (LCA).

Application to multiple-input signature analysis registers and linear cellular automata

Figure 4 shows a multiple-input signature analysis register (MISR) with a linear feedback function. The next-state matrix has the following form:

$$\mathbf{C} = \begin{bmatrix} c_1 & c_2 & c_3 & \dots & c_{k-1} & c_k \\ 1 & 0 & 0 & & 0 & 0 \\ 0 & 1 & 0 & & 0 & 0 \\ 0 & 0 & 1 & & 0 & 0 \\ & \dots & & & & \\ 0 & 0 & 0 & \dots & 1 & 0 \end{bmatrix}.$$

The entries in the first row are the feedback coefficients. The ones in the lower main diagonal represent the shifting of data. Expanding along the last column of $\mathbf{C}$, the determinant of this matrix is always

$$|\mathbf{C}| = c_k |I_{k-1}| = c_k \cdot 1 = c_k.$$

We can thus conclude the following.

Regardless of the distribution of the error patterns [with the restriction that $0 < \Pr(E) < 1$], the asymptotic aliasing probability of a multiple-input signature analysis register of length k is always 2^{-k} , if the last bit of the register is fed back. Of course, other bits in the signature

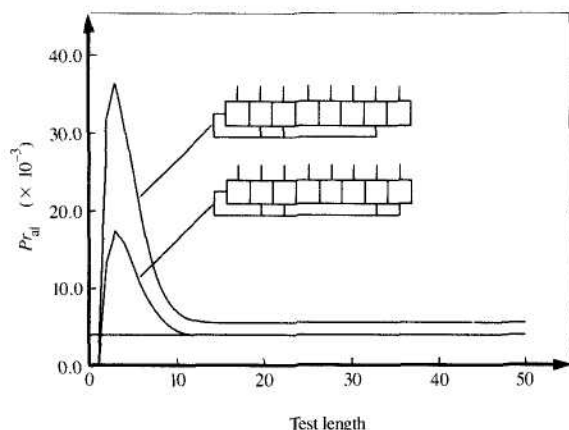


Figure 7

Impact of a missing feedback tab at the last bit of a MISR.

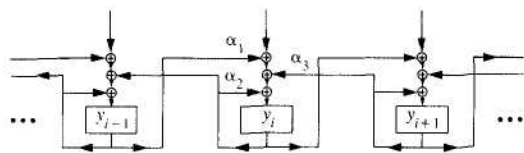


Figure 8

Linear-cellular-automata-based data compressor.

analysis register may also be fed back in addition to the k th bit.

From the work of Smith [13], it is clear that if no bits are fed back and the probability of an error is $1/2$ at each input, the final value of the aliasing probability is 2^{-k} . However, Figure 7 shows the potential impact of not feeding back the last bit of an 8-bit MISR if the probability of an error is 0.01 for all input ports of the register. The aliasing probability of the register whose last bit is not fed back may be significantly higher.

With respect to built-in test pattern generation, cellular automata have been proposed as an alternative to linear feedback shift registers [29]. Here we concentrate on the feasibility of linear cellular automata (LCA) for data-compression purposes. Figure 8 shows an example of a LCA. The state of each cell is restricted to depend only on the previous states of the cell itself, its two adjacent

Table 1 Determinants of the next-state matrix of a linear cellular automaton of length k with zero boundary conditions.

Length	C
3	α_2
4	$\alpha_2 \oplus \alpha_1 \cdot \alpha_2 \cdot \alpha_3 \oplus \alpha_1 \cdot \alpha_3$
5	$\alpha_2 \oplus \alpha_1 \cdot \alpha_2 \cdot \alpha_3$
6	$\alpha_2 \oplus \alpha_1 \cdot \alpha_2 \cdot \alpha_3 \oplus \alpha_1 \cdot \alpha_3$
7	α_2
8	$\alpha_2 \oplus \alpha_1 \cdot \alpha_3$
k	$ C_{\text{order } k} = C_{\text{order } k-6} $ $C_k = \alpha_2 \cdot C_{k-1} \oplus \alpha_1 \cdot \alpha_3 \cdot C_{k-2}$

cells, and the value of the actual input bit (Figure 8).

Generally the next-state function of each cell of a LCA can be written as

$$y_i(t) = \alpha_1 \cdot y_{i-1}(t-1)$$

$$\oplus \alpha_2 \cdot y_i(t-1) \oplus \alpha_3 \cdot y_{i+1}(t-1) \oplus x_i(t).$$

Assuming zero boundary conditions, i.e.,

$$y_0(t) = 0 \text{ and } y_{k+1}(t) = 0 \text{ for all } t,$$

the operation of a LCA-based data compressor is described by the following next-state matrix (which is tridiagonal):

$$C = \begin{bmatrix} \alpha_2 & \alpha_3 & 0 & \cdots & 0 & 0 \\ \alpha_1 & \alpha_2 & \alpha_3 & \cdots & 0 & 0 \\ 0 & \alpha_1 & \alpha_2 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & & \alpha_2 & \alpha_3 \\ 0 & 0 & 0 & & \alpha_1 & \alpha_2 \end{bmatrix}.$$

Table 1 lists the determinants for different lengths k of the data compressor. In contrast to MISRs, no simple general rule can be given for the proper selection of the next-state function of a cell. Setting $(\alpha_1, \alpha_2, \alpha_3) = (1, 1, 1)$ results in a minimal steady-state value of the aliasing probability $Pr_{al} = 2^{-k}$ for a 7-bit data compressor. However, for an 8-bit device $(\alpha_1, \alpha_2, \alpha_3) = (1, 0, 1)$ is the better choice. Figure 9 compares 8-bit data compressors with $(\alpha_1, \alpha_2, \alpha_3) = (1, 1, 1)$ and $(\alpha_1, \alpha_2, \alpha_3) = (1, 0, 1)$. The probability of any bit being in error has been set to 0.1 for all inputs.

Nonergodic Markov processes

In the previous sections the ergodic property of the Markov process has been ensured by the requirement that the probability of all input error patterns must be greater than zero. Thus, there is always a path in the state diagram between arbitrary pairs of states. However, if a fault is always propagated to a subset of the outputs of the network under test or creates 100% correlation

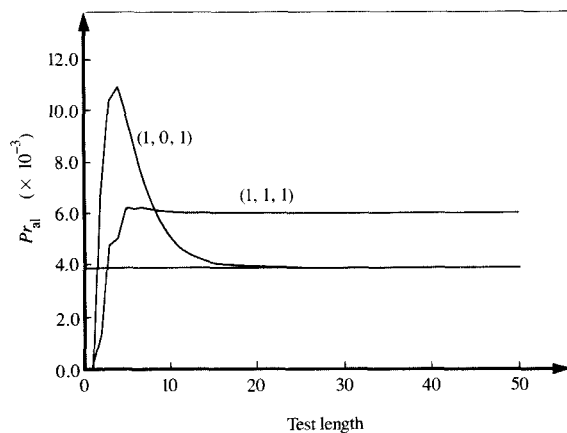


Figure 9

Aliasing probability for 8-bit cellular-automata-based data compressors with next-state coefficients $(\alpha_1, \alpha_2, \alpha_3) = (1, 1, 1)$ and $(\alpha_1, \alpha_2, \alpha_3) = (1, 0, 1)$.

conditions between any two outputs, some error patterns E will never be created, and thus can never be applied to the data compressor. Consequently, the number of possible state transitions is reduced, and we can no longer be certain that a path between two arbitrary states exists. Hence, the Markov process may become nonergodic.

Figure 10 shows the state diagram for a 3-bit multiple-input signature analysis register when a fault is propagated to input 2 of the register only. The only error patterns that are possible are $(0, 0, 0)$ and $(0, 1, 0)$, the former being the error-free good-machine response.

Starting in state $(0, 0, 0)$, only three additional states can be reached. Thus, after a sufficient number of error patterns $E(t)$ have been applied, the state probabilities of these four states can be expected to be $1/4$, while the state probabilities of the remaining states will be 0. The final value of the aliasing probability will be 2^{-2} , not 2^{-3} as is usually expected for a 3-bit signature analysis register.

Figure 11 shows the result of a simulation of the Markov process for $e_1 = e_3 = 0$ and $Pr(e_2 = 1) = 0.9$.

Figure 12 shows the state diagram of the previous multiple-input signature analysis register for the case in which an error always appears at register inputs 1 and 3 simultaneously. Now only $(0, 0, 0)$ and $(1, 0, 1)$ are possible error inputs to the data compressor. As in the previous case, the final value of the aliasing probability will be 2^{-2} instead of 2^{-3} (**Figure 13**).

Operational analysis of the data compressor

To derive criteria for checking whether the Markov process is ergodic, we now analyze how an error sequence

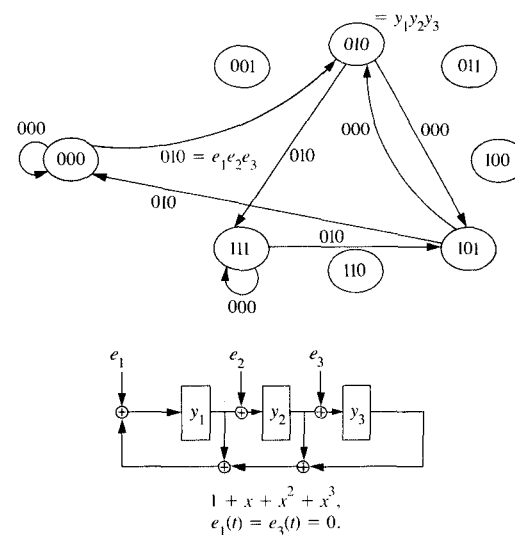


Figure 10

Nonergodic Markov process for register $1 + x + x^2 + x^3$.

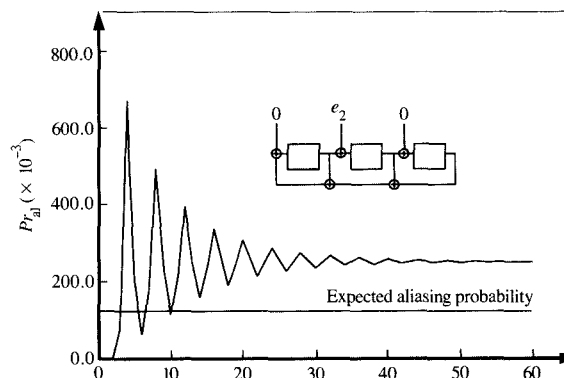


Figure 11

Aliasing in a 3-bit MISR with only one error input e_2 .

$E(t)$ is mapped onto a state sequence $Y(t)$ by a given linear data compressor. This analysis will enable us to determine the number of states of the compressor if only a subset of all possible error patterns can be applied to the inputs of the automaton. We will thus be able to determine whether the Markov process is ergodic.

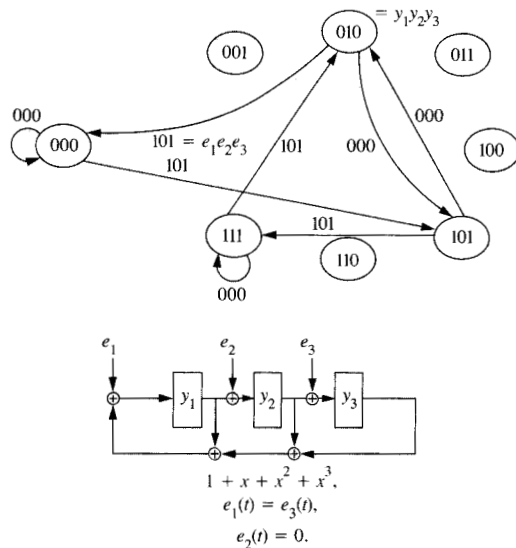


Figure 12

Nonergodic behavior of a 3-bit MISR for error patterns (0, 0, 0) and (1, 0, 1).

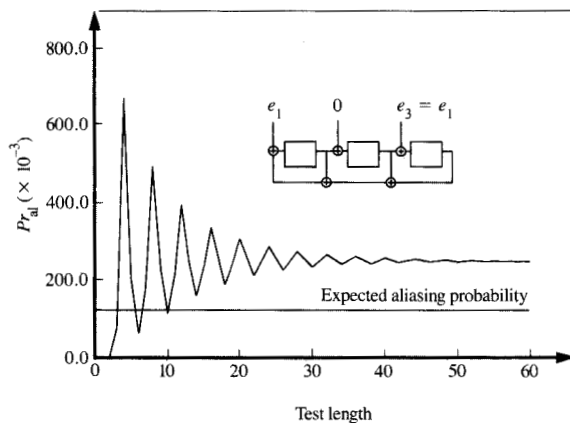


Figure 13

Increase of the aliasing probability of a 3-bit MISR due to strong correlation between e_1 and e_3 .

The analysis employed uses the D -transform [27], which is very similar to the z -transform of sampled data theory [27, 30]. However, as we are dealing with Galois functions rather than real-valued functions, it is less

Table 2 D -transform pairs.

Operation	$g(t)$	$D[g(t)]$
1. Addition	$g_1(t) \oplus g_2(t)$	$G_1(D) \oplus G_2(D)$
2. Constant multiplication	$\beta \cdot g(t)$	$\beta \cdot G(D)$
3. Sum	$\sum_{n=0}^t g(n)$	$\frac{G(D)}{1 \oplus D}$
4. Convolution	$\sum_{k=0}^t g_2(k) \cdot g_1(t-k)$	$G_1(D) \cdot G_2(D)$
5. Multiplication by	$\beta^t \cdot g(t)$	$G(\beta D)$
6. Delay	$g(t-n)$	$D^n \cdot G(D)$
7. Advance	$g(t+1)$	$D^{-1} \cdot [G(D) - g(0)]$

confusing if we differentiate between the two types of transforms.

The D -transform is defined only for functions $g(t)$ that are zero for $t < 0$:

$$D[g(t)] \equiv G(D) = g(0) \oplus D \cdot g(1) \oplus \dots$$

$$= \sum_{t=0}^{\infty} g(t) \cdot D^t.$$

Table 2 shows some transform pairs. Assuming again that the good-machine response $X(t)$ is zero, the behavior of the linear data compressor is described in the time domain by the following equation:

$$Y(t) = C \cdot Y(t-1) \oplus E(t).$$

By applying the D -transform, we get

$$D[Y(t)] = C \cdot D[Y(t-1)] \oplus D[E(t)],$$

$$Y(D) = C \cdot D \cdot Y(D) \oplus E(D).$$

Solving for $Y(D)$, an operational relationship is established between the error sequence E and the state sequence Y :

$$Y(D) = (I \oplus D \cdot C)^{-1} \cdot E(D).$$

With

$$(I \oplus DC)^{-1} = [(I \oplus DC)^{\text{adj}}]^T / (I \oplus DC)$$

$$= [(I \oplus DC)^{\text{adj}}]^T / p(D)$$

$$\equiv T(D),$$

we get

$$Y(D) = T(D) \cdot E(D).$$

Defined as

$$p(D) = |I \oplus D \cdot C|,$$

$p(D)$ is the characteristic polynomial of the next-state matrix C . $T(D)$ is the transfer function of the data compressor. Since the data compressor has several inputs and several state bits, $T(D)$ is a matrix of fractional rational functions. Hence,

$$\begin{aligned} y_1(D) &= \frac{p_{11}(D)}{p(D)} \cdot e_1(D) \oplus \frac{p_{21}(D)}{p(D)} \cdot e_2(D) \cdots \oplus \frac{p_{k1}(D)}{p(D)} \cdot e_k(D), \\ y_2(D) &= \frac{p_{12}(D)}{p(D)} \cdot e_1(D) \oplus \frac{p_{22}(D)}{p(D)} \cdot e_2(D) \cdots \oplus \frac{p_{k2}(D)}{p(D)} \cdot e_k(D), \\ &\vdots \\ y_k(D) &= \frac{p_{1k}(D)}{p(D)} \cdot e_1(D) \oplus \frac{p_{2k}(D)}{p(D)} \cdot e_2(D) \cdots \oplus \frac{p_{kk}(D)}{p(D)} \cdot e_k(D). \end{aligned}$$

For the 3-bit multiple-input signature analysis register shown in Figure 12, we obtain the following input-state relation:

$$\begin{aligned} y_1(D) &= \frac{1}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_1(D) \oplus \frac{D \cdot (D \oplus 1)}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_2(D) \oplus \frac{D}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_3(D), \\ y_2(D) &= \frac{D}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_1(D) \oplus \frac{(D \oplus 1)}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_2(D) \oplus \frac{D^2}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_3(D), \\ y_3(D) &= \frac{D^2}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_1(D) \oplus \frac{D \cdot (D \oplus 1)}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_2(D) \oplus \frac{D^2 \oplus D \oplus 1}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_3(D). \end{aligned}$$

Now we are able to analyze the behavior of a linear data compressor if only a subset of all error patterns $E(t)$ can be applied to the inputs of the compressor. Clearly, such a subset always contains the all-zero (defect-free) error pattern. Moreover, with respect to the ergodicity of the Markov process, subsets of only two patterns have to be considered, as is shown next.

Theorem 5

If, for an arbitrary subset of the input alphabet, the states of the automaton are strongly connected (no disjoint subgraphs), the state diagram will not be partitioned into disjoint subgraphs if additional symbols are added to the input alphabet.

Proof Assume a strongly connected machine with an input alphabet E and a set of states $Y = Y_1, Y_2, \dots, Y_k$. If the machine is strongly connected, there is always a sequence $E_1, E_2, \dots, E_k$ for every path from an arbitrary state Y_i to another state Y_j . If the input alphabet is increased ($E'' = E \cup E'$), the former sequence still constitutes a path from state Y_i to Y_j . The states are thus still strongly connected.

With respect to the ergodicity of the Markov process, this means that the process is ergodic if the Markov process is ergodic for a subset of the error symbols consisting of the all-zero vector and an arbitrary error vector $(e_1, e_2, \dots, e_k)$. Thus, the Markov process is ergodic for all sets of two or more error symbols that contain the all-zero vector.

In the example of Figure 11, an error was supposed to occur only at input e_2 of the investigated MISR. The set of possible error patterns consists only of the two vectors $(0, 0, 0)$ and $(0, 1, 0)$. Here the transfer function $E(D) \rightarrow Y(D)$ is described as follows:

$$\begin{aligned} y_1(D) &= \frac{D \cdot (D \oplus 1)}{D^3 \oplus D^2 \oplus D \oplus 1} \cdot e_2(D) = \frac{D \cdot (D \oplus 1)}{(D \oplus 1)^3} \cdot e_2(D) = \frac{D}{D^2 \oplus 1} \cdot e_2(D), \\ y_2(D) &= \frac{D \oplus 1}{(D \oplus 1)^3} \cdot e_2(D) = \frac{1}{D^2 \oplus 1} \cdot e_2(D), \\ y_3(D) &= \frac{D \cdot (D \oplus 1)}{(D \oplus 1)^3} \cdot e_2(D) = \frac{D}{D^2 \oplus 1} \cdot e_2(D). \end{aligned}$$

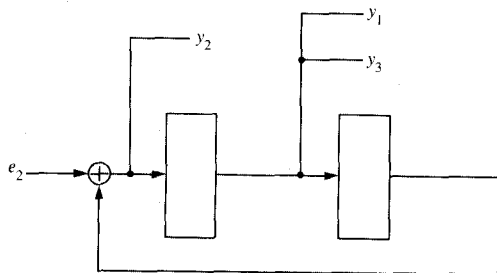


Figure 14

Functionally equivalent circuit for the 3-bit MISR if $e_1 = e_3 = 0$.

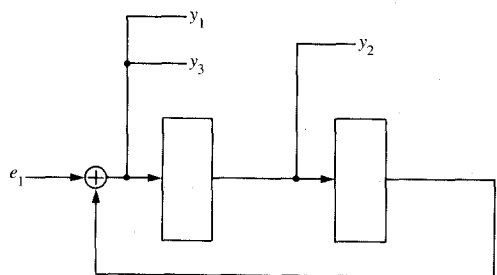


Figure 15

Functionally equivalent circuit for $E(t) \in \{(0, 0, 0), (1, 0, 1)\}$.

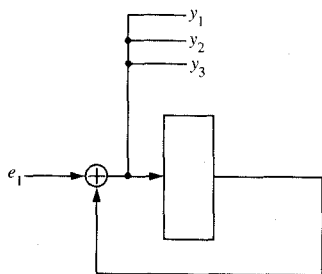


Figure 16

Functionally equivalent circuit for $E(t) \in \{(0, 0, 0), (1, 1, 1)\}$.

In the above example, the transfer function can be simplified, because the terms in the numerator and the characteristic polynomial in the denominator have a common factor. A canonical implementation of a network realizing the transfer function can easily be given. The necessary number of register cells equals the degree of the polynomial in the denominator, which is reduced from 3 to 2 in this case (**Figure 14**).

Since the state variables y_1, y_2, y_3 are derived from a smaller number of state variables y'_1, y'_2 of the equivalent network, they must be linearly dependent. Further, if a linear data compressor of length k can be modeled by an equivalent linear data compressor of length $m < k$ in the case of a reduced-error-input alphabet, the final value of the aliasing probability of the original data compressor of length k is $Pr_{al} = 2^{-m} > 2^{-k}$. **Figure 15** shows the equivalent circuit for the example of **Figure 12**, where $E \in \{(0, 0, 0), (1, 0, 1)\}$.

For the investigated 3-bit MISR, the functionally equivalent circuit has a minimal number of register cells if a fault always propagates to all three inputs of the device ($e_1 = e_2 = e_3$). In this case, we get the following transfer function:

$$y_1(D) = \frac{1 \oplus D^2}{(1 \oplus D)^3} \cdot e_1(D) = \frac{1}{1 \oplus D} \cdot e_1(D),$$

$$y_2(D) = \frac{1 \oplus D^2}{(1 \oplus D)^3} \cdot e_1(D) = \frac{1}{1 \oplus D} \cdot e_1(D),$$

$$y_3(D) = \frac{1 \oplus D^2}{(1 \oplus D)^3} \cdot e_1(D) = \frac{1}{1 \oplus D} \cdot e_1(D).$$

Figure 16 shows the equivalent circuit. An aliasing probability of 0.5 has been verified by simulation of the Markov process (**Figure 17**).

Aliasing probability and characteristic polynomial

As shown in the previous section, a reduction of the input alphabet of the data compressor may result in a partitioning of the set of states that can be visited. This partitioning is such that there exists no path in the state diagram between two states that belong to different partitions. As a result, the Markov process becomes nonergodic. Unless we are interested in autonomous behavior, a minimal subset of the input alphabet of the data compressor comprises two patterns. In this context, one of the patterns is the all-zero vector $[0, 0, \dots, 0]^T$, and the other one is $[h_1, h_2, \dots, h_k]^T$, which has its ones (and zeros) at fixed bit positions through the duration of the experiment. These two vectors can be represented by

$$E(t) = [h_1, h_2, \dots, h_k] \cdot e(t) \quad \text{with } e(t) \in \{0, 1\}.$$

Using the D -transform, the behavior of the circuit in this special situation can be analyzed as follows:

$$\begin{aligned} Y(D) &= T(D) \cdot E(D) \\ &= T(D) \cdot [h_1, h_2, \dots, h_k]^T \cdot \mathbf{D}[e(t)] \\ &= T(D) \cdot [h_1, h_2, \dots, h_k]^T \cdot e(D). \end{aligned}$$

These transfer functions are linear combinations of the elements in the respective columns of $T(D)$. If the numerator and the denominator of the resulting transfer function have common factors, the expression can be simplified, and a less complex transfer function is obtained (see previous examples):

$$\begin{bmatrix} y_1(D) \\ y_2(D) \\ \vdots \\ y_k(D) \end{bmatrix} = \begin{bmatrix} \frac{p_1(D)}{p'(D)} \\ \frac{p_2(D)}{p'(D)} \\ \vdots \\ \frac{p_k(D)}{p'(D)} \end{bmatrix} \cdot e(D).$$

Now let us assume that we get the same denominator $p'(D)$ for all transfer functions $e(D) \rightarrow y_i(D)$, $1 \leq i \leq k$. Using the transfer functions, it is now possible to obtain a canonical implementation, i.e., a network with a minimal number of register cells. The network is a single-input signature analysis register with $\deg[p'(D)]$ register cells. This kind of data compressor has been investigated in a previous paper; we refer to the results without proof [25].

For a linear data compressor with an input alphabet restricted to two symbols, the following statements are valid:

- The final value of the aliasing probability is 2^{-m} , with $m = \deg[p'(D)]$ and $p'(D)$ constituting the feedback function of the functionally equivalent canonical network.
- The aliasing probability $Pr_{al}(t)$ converges fastest to its final value if $p'(D)$ is primitive [16, 20, 31, 32].

As $p'(D)$ is always a factor of the characteristic polynomial $p(D)$ of the linear data compressor, an upper bound of the final value of the aliasing probability can be given.

Let

$$p(D) = p_1(D) \cdot p_2(D) \cdot \dots \cdot p_j(D),$$

with

$$p_i(D) \neq 1 \quad i = 1, 2, \dots, j,$$

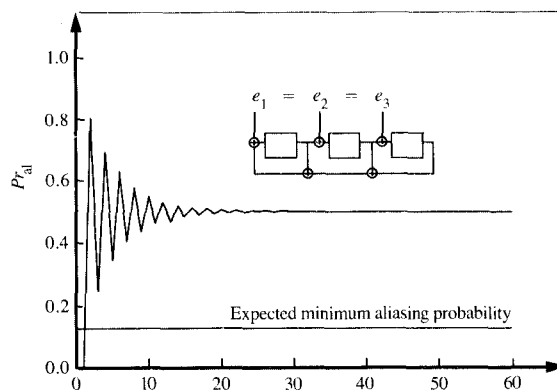


Figure 17

Aliasing probability for strongly correlated error patterns.

and

$$k_{\min} = \min_i \{\deg[p_i(D)]\} \quad i = 1, 2, \dots, j;$$

then

$$Pr_{al, \max} = 2^{-k_{\min}}$$

is an upper bound on the final value of the aliasing probability of the linear data compressor.

Figure 18 shows a MISR with feedback function $1 + x^k$ as proposed in [12]. The characteristic polynomial for this circuit is

$$p(D) = 1 \oplus D^k = (1 \oplus D)(1 \oplus D \oplus D^2 \oplus \dots \oplus D^{k-1}).$$

An upper bound of the final value of the aliasing probability for this would be

$$Pr_{al, \max} = 2^{-\deg(1 \oplus D)} = 0.5.$$

If at time t an error propagates to all inputs of the MISR, we get exactly this value of the aliasing probability (see Figure 18), regardless of the length of the register.

Now let us assume that $p(D)$ is irreducible.

Theorem 6

If the characteristic polynomial of the next-state matrix C of a linear data compressor with k register cells is irreducible, and if the input alphabet consists of two (or more) error symbols, the aliasing probability is 2^{-k} .

Proof From the transfer function of the data compressor, a functionally equivalent single-input

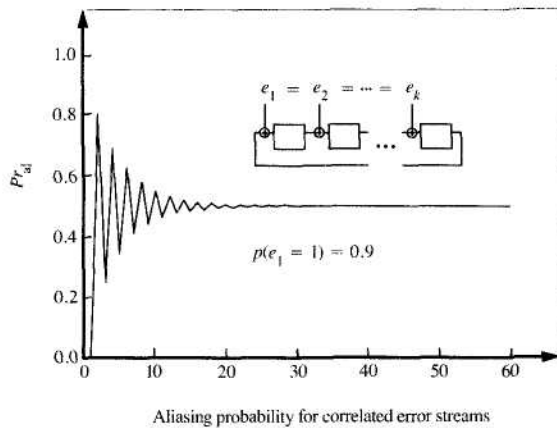


Figure 18

Worst-case aliasing probability for MISR $x^k + 1$.

signature analysis register implementation with no less than k register cells can be derived. The aliasing probability for this register is 2^{-k} , and because of the functional equivalence, the aliasing probability of the original data compressor must be 2^{-k} as well.

Corollary The aliasing probability of a linear data compressor with k register cells is 2^{-k} regardless of the probability distribution of the error pattern $Pr(E)$, if $|C| = 1$ and if the characteristic polynomial of the next-state matrix C ,

$$p(D) = |I \oplus D \cdot C|,$$

is irreducible.

Proof As has already been shown, $|C| = 1$ means that the transition matrix of the Markov process is doubly stochastic. If $p(D)$ is irreducible, the Markov process is ergodic for an arbitrary two-symbol-input alphabet that includes the all-zero vector; and with Theorem 5, the Markov process must be ergodic for any subset of the full-input alphabet, which again includes the all-zero vector. Hence, $Pr_{al} = 2^{-k}$.

Classification of linear data compressors

On the basis of the results presented here, the following classification scheme for linear data compressors can be given:

1. $|C| = 0$:

The final value of the aliasing probability depends on

the probability of an error at the outputs of the circuit under test.

2. $|C| = 1$ and $p(D)$ reducible:

The final value of the aliasing probability does not depend on the error probability, but rather on the correlation of error streams at different inputs of the data compressor and on the inputs of the compressor where the errors are observed: $Pr_{al} \leq 2^{-k_{min}}$.

3. $|C| = 1$ and $p(D)$ irreducible:

The final value of the aliasing probability of a linear data compressor with k register cells is $Pr_{al} = 2^{-k}$, with no regard to the probability distribution $Pr(E)$ of the error patterns $E(t)$.

In a recent paper [31] it has been shown, for multiple-input signature analysis registers with independent

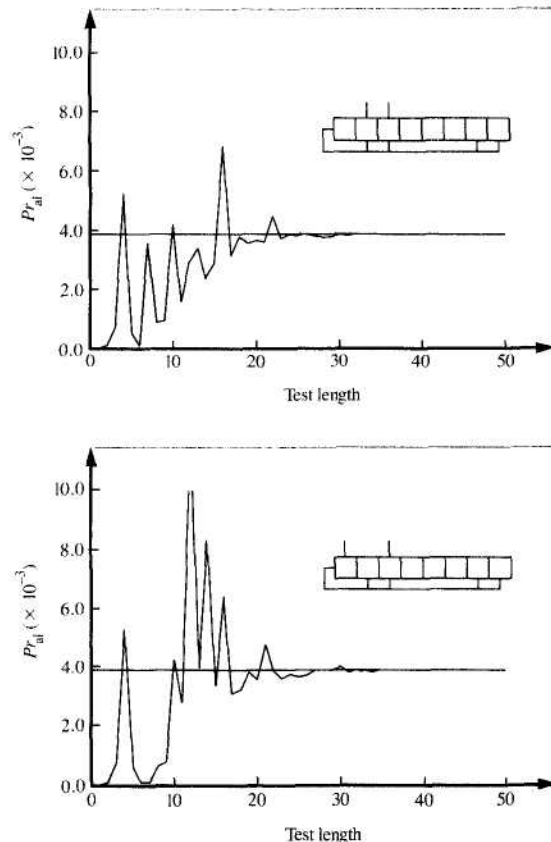


Figure 19

Impact of the error sequence on the transient of the aliasing probability of an 8-bit MISR.

inputs, that the transient of the aliasing probability has a maximum damping if the feedback polynomial is not only irreducible but primitive. As we are capable of constructing a functionally equivalent shift-register implementation by means of the D -transform, this result can be extended to the more general class of linear data compressors investigated here.

4. $|C| = 1$ and $p(D)$ primitive:

The aliasing probability converges fastest to its final value, 2^{-k} .

Simulation results show that the final value of the aliasing probability is reached after some oscillations. The magnitude of the oscillations and the locations of the local minima depend on the error pattern sequence. **Figure 19** shows the aliasing probability for an 8-bit MISR for two different fault situations. In the first case, a fault is propagated to inputs 2 and 3 simultaneously; in the second case, an error appears at register inputs 1 and 3 with probability 0.9. Since the error sequence depends on the actual fault inside the circuit, no advantage can be drawn from knowing the minima for a particular fault situation. A low final value of the aliasing probability, together with a strong damping of the transient, has to be considered as the best overall choice.

Application to multiple-input signature analysis registers

In this section we investigate the relation between the feedback function and the characteristic polynomial $p(D)$. The feedback function is usually given as a polynomial,

$$p(x) = 1 \oplus \sum_{j=1}^k c_j \cdot x^j.$$

The coefficients c_j are identical to the first row of the next-state matrix C , and the ones in the lower main diagonal represent the shifting of data (Figure 4).

The characteristic polynomial $p(D)$ is

$$p(D) = |I \oplus D \cdot C| = \begin{vmatrix} c_1 \cdot D \oplus 1 & c_2 \cdot D & c_3 \cdot D & \cdots & c_{k-1} \cdot D & c_k \cdot D \\ D & 1 & 0 & \cdots & 0 & 0 \\ 0 & D & 1 & \cdots & 0 & 0 \\ & & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & 0 & \cdots & D & 1 \end{vmatrix}.$$

$$p(D) = 1 \oplus \sum_{j=1}^k c_j \cdot D^j.$$

Because the characteristic polynomial $p(D)$ is identical to the feedback polynomial $p(x)$, we can conclude the following:

If the feedback polynomial of a multiple-input signature analysis register of length k is irreducible, the final value of the aliasing probability is 2^{-k} .

For a list of primitive polynomials up to degree 300, see [10].

Application to linear cellular automata

For the given class of LCAs, the characteristic polynomial is the following determinant:

$$p(D) = |I + D \cdot C| = \begin{vmatrix} \alpha_2 \cdot D \oplus 1 & \alpha_3 \cdot D & 0 & \cdots & 0 & 0 \\ \alpha_1 \cdot D & \alpha_2 \cdot D \oplus 1 & \alpha_3 & \cdots & 0 & 0 \\ 0 & \alpha_1 \cdot D & \alpha_2 \cdot D \oplus 1 & \cdots & 0 & 0 \\ & & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & \cdots & \alpha_2 \cdot D \oplus 1 & \alpha_2 \cdot D \\ 0 & 0 & 0 & \cdots & \alpha_1 & \alpha_2 \cdot D \oplus 1 \end{vmatrix}.$$

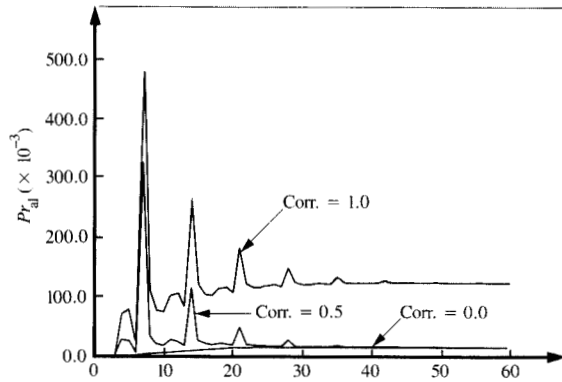


Figure 20

Impact of correlation on the aliasing probability of a 6-bit LCA.

Coefficients α_1 , α_3 , and α_2 determine whether the state of the left neighbor, the cell itself, or the state of the right neighbor is taken into account in the calculation of the next state of a cell. Table 3 lists the characteristic polynomials for linear cellular automata with zero boundary condition through length 9.

None of the polynomials listed in Table 3 is irreducible. Thus, we can conclude that for register lengths <10 , multiple-input signature analysis registers are superior to these linear cellular automata with respect to aliasing in the data compression mode. Since a MISR with an aliasing probability of 2^{-k} , which is minimal for the investigated class of linear machines, exists for every register length, MISRs are more universal than LCAs. Figure 20 shows the aliasing probability of this 6-bit LCA, $(\alpha_1, \alpha_2, \alpha_3) = (1, 1, 1)$. The error is assumed to propagate with probability 0.9 to inputs 3 and 4 of the data compressor. If the error streams are perfectly correlated, the aliasing probability becomes $2^{-3} > 2^{-6}$ (Figure 20).

Impact of time correlation

In the previous section, correlation has always been considered as a dependency between different bits e_i of the error input vector $E(t)$. Let us now take a short look at how correlation between successive error bits at one bit position might influence aliasing. It has been shown that a linear feedback shift register, which is a functionally equivalent canonical representation of the linear data compressor, can be derived by means of the D -transform analysis. Thus, we can rely on previous results [10, 11, 13, 17, 32] and state the following:

An aliasing error due to time correlation of error bits occurs only if the D -transformed error vector sequence is a multiple of the characteristic polynomial of the linear data compressor.

There are more complex correlations, combinations of time and space correlations, possible for MISRs. For instance, error cancellation occurs for the 3-bit MISR of Figure 12, if inputs $e_2 = e_3 = e$, and input $e_1 = D^2e$, i.e., 100% correlated to e but delayed two time units. Then,

$$y_1(D) = 0,$$

$$y_2(D) = e(D),$$

and

$$y_3(D) = (D + 1)e.$$

Thus

$$y_1(t) = 0,$$

$$y_2(t) = e(t),$$

and

$$y_3(t) = e(t) \oplus e(t - 1).$$

Then the final probability of aliasing is $(1 - p) \cdot [(1 - p)^2 \oplus p^2]$, or 0.25 for $p = 0.5$.

On the other hand, for the correlation example of Figure 12,

$$y_1(D) = y_2(D) = y_3(D) = \frac{1}{1 \oplus D} \cdot e_1(D).$$

Table 3 Characteristic polynomial for linear cellular automata.

Length	Characteristic polynomial
3	$(\alpha_2 \cdot D \oplus 1)^3$
4	$(\alpha_2 \cdot D \oplus 1)^4 \oplus \alpha_1 \cdot \alpha_3 \cdot D \cdot (\alpha_2 \cdot D \oplus 1)^2 \oplus \alpha_1 \cdot \alpha_3 \cdot D^4$
5	$(\alpha_2 \cdot D \oplus 1) \cdot [(\alpha_2 \cdot D \oplus 1)^4 \oplus \alpha_1 \cdot \alpha_3 \cdot D^4]$
6	$(\alpha_2 \cdot D \oplus 1)^6 \oplus \alpha_1 \cdot \alpha_3 \cdot D^2 \cdot (\alpha_2 \cdot D \oplus 1)^4 \oplus \alpha_1 \cdot \alpha_3 \cdot D^6$
7	$(\alpha_2 \cdot D \oplus 1)^7$
8	$(\alpha_2 \cdot D \oplus 1)^8 \oplus \alpha_1 \cdot \alpha_3 \cdot D^2 \cdot (\alpha_2 \cdot D \oplus 1)^6 \oplus \alpha_1 \cdot \alpha_3 \cdot D^4 \cdot (\alpha_2 \cdot D \oplus 1)^4 \oplus \alpha_1 \cdot \alpha_3 \cdot D^8$
9	$(\alpha_2 \cdot D \oplus 1) \cdot [(\alpha_2 \cdot D \oplus 1)^8 \oplus \alpha_1 \cdot \alpha_3 \cdot D^4 \cdot (\alpha_2 \cdot D \oplus 1)^4 \oplus \alpha_1 \cdot \alpha_3 \cdot D^8]$

$$p_k(D) = (\alpha_2 \cdot D \oplus 1) \cdot p_{k-1}(D) \oplus \alpha_1 \cdot \alpha_3 \cdot D^2 \cdot p_{k-2}(D)$$

Then, taking the inverse D -transform,

$$y_i(t) = \sum_{t=0}^n e_i(t), \quad i = 1, 2, 3.$$

Thus, for large n , the final aliasing probability is $1/2$, since it reflects the cumulative parity of the incoming error stream. On average, this signature will be zero (aliasing) 50% of the time.

Conclusions

In this paper the aliasing probability of multiple-input linear data compressors has been investigated; sufficient conditions have been derived to ensure an aliasing probability of 2^{-k} if the data compressor has k register cells. If these conditions are met, the aliasing probability does not depend on the distribution of the errors at the data compressor input. In particular, the aliasing probability does not depend on correlation between errors at the different inputs. By application of the derived criteria, it has been shown that multiple-input signature analysis registers with an irreducible feedback polynomial can meet the conditions for every register length.

References

1. A. Frohwerk, "Signature Analysis: A New Digital Field Service Method," *Hewlett-Packard J.*, pp. 2-8 (May 1977).
2. J. P. Hayes, "Check Sum Test Methods," *Proceedings of the Fault-Tolerant Computing Symposium (FTCS-6)*, Pittsburgh, June 1976, pp. 114-119.
3. J. Savir, "Syndrome-Testable Design of Combinational Circuits," *IEEE Trans. Computers* C-29, 442-451 (June 1980).
4. A. K. Susskind, "Testing by Verifying Walsh Coefficients," *Proceedings of FTCS-11*, June 1981, pp. 206-208.
5. R. David, "Testing by Feedback Shift Registers," *IEEE Trans. Computers* C-29, 669-673 (July 1980).
6. K. P. Parker, "Compact Testing: Testing with Compressed Data," *Proceedings of FTCS-6*, Pittsburgh, June 1976, pp. 93-98.
7. W. C. Carter, "The Ubiquitous Parity Bit," *Proceedings of FTCS-12*, Portland, OR, June 1982.
8. B. Könemann, J. Mucha, and G. Zwiehoff, "Built-In Test for Complex Digital Integrated Circuits," *IEEE J. Solid-State Circuits* SC-15, 315-319 (June 1980).
9. Z. Barzilai, J. Savir, G. Markowsky, and M. G. Smith, "The Weighted Syndrome Sums Approach to VLSI Self-Testing," *IEEE Trans. Computers* C-30, 190-194 (February 1981).
10. P. H. Bardell, W. H. McAnney, and J. Savir, *Built-In Test for VLSI*, John Wiley & Sons, Inc., New York, 1987.
11. T. W. Williams, *VLSI Testing*, Elsevier Science Publishers B.V., Amsterdam, Netherlands, 1986.
12. R. David, "Feedback Shift Register Testing," *Proceedings of FTCS-8*, Toulouse, France, June 1978, pp. 103-107.
13. J. E. Smith, "Measures of the Effectiveness of Fault Signature Analysis," *Proceedings of the 1980 IEEE International Test Conference*, pp. 510-514.
14. T. W. Williams, W. Daehn, M. Gruetzner, and C. W. Starke, "Comparison of Aliasing Errors for Primitive and Non-Primitive Polynomials," *Proceedings of the 1986 IEEE International Test Conference*, pp. 282-288.
15. D. Bhavsar and B. Krishnamurthy, "Can We Eliminate Fault Escapes in Self-Testing by Polynomial Division (Signature Analysis)?" *Proceedings of the 1984 IEEE International Test Conference*, pp. 134-139.
16. T. W. Williams, W. Daehn, M. Gruetzner, and C. W. Starke, "Aliasing Errors in Signature Analysis Registers," *IEEE Design & Test of Computers* 4, 39-45 (April 1987).
17. A. Ivanov and V. K. Agarwal, "On a Fast Method to Monitor the Behaviour of Signature Analysis Register," *Proceedings of the 1987 IEEE International Test Conference*, pp. 645-655.
18. A. Ivanov and V. K. Agarwal, "An Iterative Technique for Calculating the Aliasing Probability of Linear Feedback Signature Registers," *Proceedings of FTCS-18*, June 1988, pp. 70-75.
19. E. J. McCluskey, "Built-In Self Test Techniques," *IEEE Design & Test of Computers* 2, 21-28 (April 1985).
20. T. W. Williams, W. Daehn, M. Gruetzner, and C. W. Starke, "Aliasing Errors with Primitive and Non-Primitive Polynomials," *Proceedings of the 1987 IEEE International Test Conference*, pp. 637-644.
21. M. Damiani, P. Olivo, M. Favalli, and B. Riccò, "An Analytical Model for the Aliasing Probability in Signature Analysis Testing," *IEEE Trans. Computer Aided Design* 8, 1133-1144 (1989).
22. S. K. Gupta and D. K. Pradhan, "A New Framework for Designing and Analyzing BIST Techniques: Computation of Exact Aliasing Probability," *Proceedings of the 1988 IEEE International Test Conference*, pp. 329-342.
23. R. David, "Signature Analysis of Multi-Output Circuits," *Proceedings of FTCS-14*, Orlando, June 1984, pp. 366-371.
24. T. W. Williams and W. Daehn, "Aliasing Errors in Multiple Input Signature Analysis Registers," *Proceedings of the 1st European Test Conference*, Paris, April 12-14, 1989, pp. 338-345.
25. T. W. Williams and W. Daehn, "Aliasing Probability for Multiple Input Signature Analyzers with Dependent Inputs," *Proceedings of CompEuro 89*, Hamburg, FRG, May 8-12, 1989, pp. 5-120-5-127.
26. A. Hławiczka, "Hybrid Design of Parallel Signature Analyzers," *Proceedings of the 1st European Test Conference*, Paris, France, April 12-14, 1989, pp. 354-360.
27. T. L. Booth, *Sequential Machines and Automata Theories*, John Wiley & Sons, Inc., New York, 1967.
28. W. Feller, *An Introduction to Probability Theory and Its Applications*, John Wiley & Sons, Inc., New York, 1965.
29. P. D. Hortensius, R. D. McLeod, and H. C. Card, "Cellular Automata Based Logic Block Observers," *Proceedings of the Second Technical Workshop: New Directions for IC Testing*, Winnipeg, Manitoba, Canada, April 1987, pp. 1-18.
30. A. V. Oppenheim and R. W. Schaefer, *Digital Signal Processing*, Prentice-Hall, Inc., Englewood Cliffs, NJ, 1975.
31. M. Damiani, P. Olivo, M. Favalli, S. Ercolani, and B. Riccò, "Aliasing in Signature Analysis Testing with Multiple Shift Registers," *Proceedings of the 1st European Test Conference*, Paris, April 12-14, 1989, pp. 346-353.
32. J. E. Megitt, "Error Correcting Codes and Their Implementation for Data Transmission Systems," *IRE Trans. Info. Theory* IT-7, 234-244 (1961).

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